UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,290	04/01/2004	Nobuyuki Sato	251394US2	6122

22850 7590 06/28/2005

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EV

Office Action Summary	Application No.	Applicant(s)	
	10/814,290	SATO, NOBUYUKI	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-15** are currently pending in the application.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on an application filed in JAPAN, 2004-027066 on 02/03/2004.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 08/17/2004. The references cited on the PTOL 1449 form have been considered.

Specification

The disclosure is objected to because of the following informalities:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1, 6, 8, 10 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa (USP 5,471,366) in view of Nam et al. (USP 6,756,689 hereinafter referred to as "Nam").

Regarding Claims **1, 8, 10 and 12**, Ozawa discloses in Figs. 2-3 and the corresponding texts as set forth in column 4, line 40-column 6, line 25, a semiconductor module/a multi-chip module 30 comprises:

a package substrate 31;

a plurality of semiconductor chips 32_{-1}-32_{-4} having top surfaces and back surfaces and being mounted by flip chip bonding above said package substrate while letting said top surfaces face said package substrate;

a plurality of heat sinks/thermal conductive blocks 33_{-1}-33_{-4} disposed above said back surfaces of said plurality of semiconductor chips; and

a resin member 34 configured to seal said plurality of semiconductor chips as a single package.

Ozawa fails to teach a multi-chip module comprises a plurality of power switching device chips, and a drive-use integrated circuit ("IC") chip mounted by flip chip bonding above said package substrate, configured to drive gates of transistors formed in said plurality of power switching device chips; wherein said drive-use IC chip is not covered with the heat sinks. Nam teaches that a multi-chip package in which a transistor, which is a switching device, and a control IC 16 not covered with the heat sink (Fig. 1), which is a driving device, are mounted together in a package. In power devices, a smart power switching (SPS) product contains a control IC,

which is a driving device, and a transistor, which is a switching device as set forth in column 1, lines 10-22. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teaching of a multi-chip package including a transistor, which is a driving device, and a control IC, which is a driving device, are mounted together in a package, as taught by Nam to incorporate into Ozawa's a multi-chip module to replace the semiconductor chips with a transistor, which is a switching device, and a control IC, which is a driving device in order to form a power device having multi-chip package structure.

Regarding Claim **6**, Ozawa discloses all the claimed limitations except for a respective one of said plurality of heat sinks has a one surface and a remaining surface on the opposite side thereof, said one surface facing the back surface of a corresponding one of said plurality of power switching device chips, and wherein said remaining surface is exposed to outside of said semiconductor module. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a respective one of said plurality of heat sinks having a one surface and a remaining surface on the opposite side thereof, said one surface facing the back surface of a corresponding one of said plurality of power switching device chips, and wherein said remaining surface is exposed to outside of said semiconductor module since it was known in the art that such configuration is used to enhance and to improve the heat dissipation of power switching device chips.

Claims **2-4, 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa (USP 5,471,366) in view of Nam et al. (USP 6,756,689 hereinafter referred to as "Nam") and further in view of Lai et al. (USP 6,236,568 hereinafter referred to as "Lai").

Regarding Claims **2-4**, Ozawa and Nam disclose all the claimed limitations except for the at least one of said plurality of heat sinks extends to overlie said drive-use IC chip; wherein said drive-use IC chip is less in thickness than one of said power switching device chips having its back surface on which the heat sink extending to overlie said drive-use IC chip is disposed; and wherein said heat sink extending to overlie said drive-use IC chip is flat. Lai teaches in Fig. 6 an integrated circuit package comprises an improved heat sink 116' which is unabutted on an integrated circuit chip 102', and the heat sink extending to overlie the integrated circuit chip is flat. This feature can prevent the heat sink from causing a thermal compressive stress on the integrated circuit chip during the cooling process as set forth in column 2, lines 25-34. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of an integrated circuit package comprising an improved heat sink which is unabutted on an integrated circuit chip, as taught by Lai into and modify the Ozawa and Nam's structure to include the at least one of said plurality of heat sinks extends to overlie said drive-use IC chip in order to prevent the heat sink from causing a thermal compressive stress on the drive-use IC chip during the cooling process. Lai fails to teach wherein said drive-use IC chip is less in thickness than one of said power switching device chips. It would have been an obvious matter of design choice to make said drive-use IC chip less in thickness than one of said power switching device chips, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Regarding Claim **11**, Ozawa and Nam disclose all the claimed limitations as recited in Claim **1** except for a heat sink being disposed above said back surface of said power switching

device chip and extending to overlie said driver IC chip. Lai teaches in Fig. 6 an integrated circuit package comprises an improved heat sink 116' which is unabutted on an integrated circuit chip 102', and the heat sink extending to overlie the integrated circuit chip is flat. This feature can prevent the heat sink from causing a thermal compressive stress on the integrated circuit chip during the cooling process as set forth in column 2, lines 25-34. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of an integrated circuit package comprising an improved heat sink which is unabutted on an integrated circuit chip, as taught by Lai into and modify the Ozawa and Nam's structure to include the at least one of said plurality of heat sinks extends to overlie said drive-use IC chip in order to prevent the heat sink from causing a thermal compressive stress on the drive-use IC chip during the cooling process.

Claim **5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa (USP 5,471,366) in view of Nam et al. (USP 6,756,689 hereinafter referred to as "Nam") and further in view of Kohno et al. (USP 6,259,156 hereinafter referred to as "Kohno").

Ozawa and Nam disclose all the claimed limitations except for said plurality of heat sinks are electrically connected respectively to source electrodes or drain electrodes of said back surfaces of corresponding ones of said plurality of power switching device chips and also electrically connected to terminals of said package substrate. Kohno teaches in Fig. 7 that a semiconductor device comprises a heat sink 9 is electrically connected respectively to source electrode 4 or drain electrode 3, so that the heat evolved by the active element is radiated to the heat sink of the package from the source electrode and the drain electrode to improve the heat

diffusion/dissipation efficiency (col. 4, line 35-col. 5, line 33). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of a semiconductor device comprises a heat sink is electrically connected respectively to source electrode or drain electrode, as taught by Kohno into and modify the Ozawa and Nam's structure to include said plurality of heat sinks are electrically connected respectively to source electrodes or drain electrodes of said back surfaces of corresponding ones of said plurality of power switching device chips and also electrically connected to terminals of said package substrate in order to improve the heat diffusion/dissipation efficiency.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa (USP 5,471,366) in view of Nam et al. (USP 6,756,689 hereinafter referred to as "Nam") and further in view of Kitabatake et al. (USP 6,580,125 hereinafter referred to as "Kitabatake").

Regarding Claim 7, Ozawa and Nam disclose all the claimed limitations except for gate electrodes and source electrodes are formed at said top surfaces of said plurality of power switching device chips and wherein drain electrodes are formed at said back surfaces. Kitabatake teaches that a semiconductor device, in which an insulating gate electrode and source electrodes are formed on the upper surface side of a semiconductor substrate and a drain electrode is formed on the lower surface side thereof so that a wide region in the semiconductor substrate is used for passing a large current in a vertical direction, is conventionally known as a semiconductor power device to be placed in an inverter as set forth in column 1, lines 13-20. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form gate electrodes and source electrodes are formed at said top surfaces of said plurality of

power switching device chips and wherein drain electrodes are formed at said back surfaces since it was known in the art that such configuration is conventionally known as a semiconductor power device for passing a large current in a vertical direction.

Claims **9, 13, 14 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa (USP 5,471,366) in view of Nam et al. (USP 6,756,689 hereinafter referred to as "Nam") and further in view of Shirai et al. (USP 6,806548 hereinafter referred to as "Shirai").

Ozawa and Nam disclose all the claimed limitations except for at least one of said plurality of power switching device chips has a diode as built therein, said diode being connected in parallel to one of said transistors; a DC-DC converter including said semiconductor module; a semiconductor device comprising said semiconductor module and a pulse width modulation (PWM) control IC chip configured to control driving of said gates by said drive-use IC chip; and a semiconductor device comprising a DC-DC converter including said semiconductor module, a central processing unit (CPU) to which electrical power is supplied thereto by said DC-DC converter; and another heat sink being disposed above said CPU and extending to reach a location covering said semiconductor. Shirai teaches in Figs. 1 and 19 that a semiconductor device comprises a power MISFET Q, a body diode BD, and a schottky barrier diode SBD. The body diode BD and the schottky barrier diode SBD are connected in parallel with power MISFET Q. The power MISFET is of a structure wherein plural transistor cells comprising fine patterns of MISFETS are connected in parallel to obtain a large electric power as set forth in column 8, line 65-column 9, line 10, and a conventional synchronous rectification type DC-DC converter using power MISFETs, a pulse width modulation (PWM) control IC chip, and a central

processing unit (CPU). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of semiconductor device comprises a power MISFET Q, a body diode BD, and a schottky barrier diode SBD. The body diode BD and the schottky barrier diode SBD are connected in parallel with power MISFET Q, and a conventional synchronous rectification type DC-DC converter using power MISFETs, having a pulse width modulation (PWM) control IC chip, and a central processing unit (CPU), as taught by Shirai into the Ozawa and Nam's structure and modify to arrive the claimed limitations in order to obtain a large power and to form a synchronous rectification type DC-DC converter using power MISFETs, having a pulse width modulation (PWM) control IC chip, and a central processing unit (CPU).

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

06/23/05

Andy Huynh

Patent Examiner